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EXAMINER	
PATEL, HARESH N	

ART UNIT	PAPER NUMBER
2154	

DATE MAILED: 08/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/873,038	LAL, SANJAY	
	Examiner	Art Unit	
	Haresh Patel	2154	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16,21-27 and 33-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16,21-27 and 33-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-16, 21-27 and 33-39 are presented for examination. Claims 17-20 and 28-32 are cancelled.

Response to Arguments

2. Applicant's arguments filed 6/2/2005 have been fully considered but they are not persuasive. Therefore, rejection of claims 1-16, 21-27 and 33-39 is maintained.

Applicant argues (1), "none of the cited references discloses the amended limitations, each processor running a specific operating system. The memory includes a common interrupt handling vector space shared by the multiple processors and a dedicated interrupt handling vector space for each processor respectively. When a processor receives an exception, the processor executes one or more instructions stored within the common interrupt handling vector space to determine based on the identification of the processor which of the dedicated interrupt handling vector space should be executed to handle the exception. Thereafter, the processor executes an interrupt service routine from the determined dedicated interrupt handling vector space associated with the processor, a network element for interfacing different networks, where the multi-processor system is part of a control card within the network element". The examiner respectfully disagrees in response to applicant's arguments. The limitations, "none of the cited references discloses the amended limitations, each processor running a specific operating system. The memory includes a common interrupt handling vector space shared by the multiple processors and a dedicated interrupt handling vector space for each processor respectively. When a processor receives an exception, the processor executes one or more

instructions stored within the common interrupt handling vector space to determine based on the identification of the processor which of the dedicated interrupt handling vector space should be executed to handle the exception. Thereafter, the processor executes an interrupt service routine from the determined dedicated interrupt handling vector space associated with the processor, a network element for interfacing different networks, where the multi-processor system is part of a control card within the network element", has been newly added, which is addressed by the new ground(s) of rejection (please refer to the below rejections of this office action). Therefore, the rejection is maintained.

Applicant argues (2), "cited references, i.e., Browning et al., 6,006,247, IBM (Hereinafter Browning-IBM) in view of O'Shea-Intel 6,611,911, Intel (Hereinafter O'Shea-Intel) and Endo et al., 6,615,303, Hitachi, Ltd, (Hereinafter Endo-Hitachi) are improperly combined. The examiner respectfully disagrees in response to applicant's arguments. The cited references, Browning et al., 6,006,247, IBM (Hereinafter Browning-IBM), O'Shea-Intel 6,611,911, Intel (Hereinafter O'Shea-Intel) and Endo et al., 6,615,303, Hitachi, Ltd, (Hereinafter Endo-Hitachi) teach a method, a system, a machine-readable medium for handling exceptions in a multi processing system, all what the applicant is trying to accomplish, as per the claimed invention (see claim 1). Browning-IBM teaches a method a system and a machine-readable medium that provides instructions for handling a exceptions within a processor in a multi-processing system (e.g., col., 2, lines 40 –65, col., 4, lines 6 – 22, figure 1). O'Shea-Intel teaches well-known concept of a query that is internal to the processor (e.g., col., 4, lines 1 – 18). Endo-Hitachi teaches well-known concept of executing an interrupt handler located within one of a different interrupt handling vector address spaces (e.g., figure 1). The interrupt handler would help handle the

interrupt/exception. The well-known concept of using different interrupt handlers stored in the memory would help handle different types of interrupts. The processor would help process the exceptions / interrupts using the different interrupt handlers. Hence, the combined teachings of Browning-IBM, O'Shea-Intel and Endo-Hitachi disclose all the claimed subject matter that facilitate a method, a system, a machine-readable medium for handling exceptions in a multi processing system, all what the applicant is trying to accomplish, as per the claimed invention. Also, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of a primary reference. It is also not that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinally skill in the art. In re Keller, 642 F.2d 414, 425, 208 USPQ 871, 881 (CCPA 1981); In re Young, 927 F.2d 588, 591, 18 USPQ2d 1089, 1091 (Fed. Cir. 1991). In response to applicant's argument that the examiner has combined an excessive number of references, reliance on a large number of references in a rejection does not, without more, weigh against the obviousness of the claimed invention. See *In re Gorman*, 933 F.2d 982, 18 USPQ2d 1885 (Fed. Cir. 1991). In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

The newly added limitations is addressed by the new ground(s) of rejection (please refer to the below rejections of this office action). Therefore, the rejection is maintained.

Response to Amendment

3. The amendment filed 6/2/2005 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows:

a. addition of limitations, "a dedicated interrupt handling vector address space for each of the plurality of the processors", "a respective dedicated interrupt handling vector address spaces associated with the processor", in claim 1,

b. addition of limitations, "a dedicated interrupt handling vector address spaces associated with a processor executing", in claim 3,

c. addition of limitations, "the processors transmits a signal via a respective interface to the memory controller", in claim 10,

d. addition of limitations, "the signal received from each processor", in claim 11,

e. addition of limitations, "a dedicated interrupt handling vector address spaces associated with the second processor", in claim 12,

f. addition of limitations, "a dedicated interrupt handling vector address space for each of the plurality of the processors", "a respective dedicated interrupt handling vector address spaces associated with the processor", in claim 21,

g. newly presented limitations, "a first network and a second network different that the first network", in claim 33,

h. newly presented limitations, "a first line card coupled the first network and a second line card coupled to the second network", "routing network traffic between the first and second networks via the first and second line cards respectively, in claim 34,

i. newly presented limitations, "a network provider network and a service provider network", in claims 35 and 38,

j. newly presented limitations, "routing network traffic", in claims 36 and 39,

k. newly presented limitations, "routing traffic between networks", "a respective dedicated interrupt handling vector address spaces associated with the second processor", in claim 37.

Applicant is required to cancel the new matter, to avoid abandonment of this application, in the reply to this Office Action.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Amended claims 1, 3, 10-12 and 21 and newly presented claims 33-39 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art to use and/or make the invention.

The specification does not contain subject matter to implement limitations, "a dedicated interrupt handling vector address space (single) for each of the plurality of the processors", "a respective dedicated interrupt handling vector address spaces (multiple) associated with the processor (single)", as cited in claim 1. Multiple exceptions cannot be handled by handling a single exception using multiple processors. Also, paragraph 17, page 6 of the specification, clearly reflects, usage of one vector space (single) for one processor (single) only and usage of dedicated resource is in reference to storage only (paragraph 26, page 9).

The specification does not contain subject matter to implement limitations, "a dedicated interrupt handling vector address spaces (multiple) associated with a processor (single) executing", as cited in claim 3. Also, paragraph 17, page 6 of the specification, clearly reflects, usage of one vector space (single) for one processor (single) only and usage of dedicated resource is in reference to storage only (paragraph 26, page 9).

The specification does not contain subject matter to implement limitations, "the processors (multiple) transmits a signal (single) via a respective interface to the memory controller", as cited in claim 10. Also, paragraph 17, page 6 of the specification, clearly reflects, usage of one signal (single) for one processor (single) only.

The specification does not contain subject matter to implement limitations, "the signal (single) received from each processor (multiple)", as cited in claim 11. Also, paragraph 17, page 6 of the specification, clearly reflects, usage of one signal (single) for one processor (single) only.

The specification does not contain subject matter to implement limitations, "a dedicated interrupt handling vector address spaces (single) associated with the second processor (single)",

as cited in claim 12. Also, paragraph 17, page 6 of the specification, clearly reflects, usage of one vector space (single) for one processor (single) only and usage of dedicated resource is in reference to storage only (paragraph 26, page 9).

The specification does not contain subject matter to implement limitations, "a dedicated interrupt handling vector address space (single) for each of the plurality of the processors", "a respective dedicated interrupt handling vector address spaces (multiple) associated with the processor (single)", as cited in claim 21. Also, paragraph 17, page 6 of the specification, clearly reflects, usage of one vector space (single) for one processor (single) only and usage of dedicated resource is in reference to storage only (paragraph 26, page 9).

The specification does not contain subject matter to implement limitations, "a first network and a second network different that the first network", as cited in claim 33. Also, paragraph 34, page 11 of the specification, clearly reflects, usage of different operating system can handle the same exception differently, which is not same as different networks.

The specification does not contain subject matter to implement limitations, "a first line card coupled the first network and a second line card coupled to the second network", "routing network traffic between the first and second networks via the first and second line cards respectively", as cited in claim 33. Also, paragraph 3, page 2 of the specification, clearly reflects, usage of each processor is running a different operating system in order to accommodate the various functionality required for these control cards. To help illustrate, one processor could include a real time operating system in order to handle routing of data received within the network element, while a second processor could include a non-real time operating system in order to handle provisioning and configuration of the network element. Hence, control cards are

necessary rather line cards mentioned in the claimed subject matter as there is no mention of line cards. A real time operating system is needed to handle routing. Further, routing is performed on "data received" only and not on all the traffic between networks, as traffic is not limited to "data received" only.

The specification does not contain subject matter to implement limitations, "a network provider network and a service provider network", as cited in claims 35 and 38. Also, paragraph 34, page 11 of the specification, clearly reflects, usage of different operating system can handle the same exception differently, which is not same as a network provider network and a service provider network.

The specification does not contain subject matter to implement limitations, "routing network traffic", as cited in claims 36 and 39. Also, paragraph 3, page 2 of the specification, clearly reflects, usage of each processor is running a different operating system in order to accommodate the various functionality required for these control cards. To help illustrate, one processor could include a real time operating system in order to handle routing of data received within the network element, while a second processor could include a non-real time operating system in order to handle provisioning and configuration of the network element. Hence, a real time operating system is needed to handle routing. Further, routing is performed on "data received" only and not on all the traffic between networks, as traffic is not limited to "data received" only.

The specification does not contain subject matter to implement limitations, "routing traffic between networks", "a respective dedicated interrupt handling vector address spaces (multiple) associated with the second processor (single)", as cited in claims 37. Also, paragraph

3, page 2 of the specification, clearly reflects, usage of each processor is running a different operating system in order to accommodate the various functionality required for these control cards. To help illustrate, one processor could include a real time operating system in order to handle routing of data received within the network element, while a second processor could include a non-real time operating system in order to handle provisioning and configuration of the network element. Hence, a real time operating system is needed to handle routing. Further, routing is performed on "data received" only and not on all the traffic between networks, as traffic is not limited to "data received" only. Also, paragraph 17, page 6 of the specification, clearly reflects, usage of one signal (single) for one processor (single) only and usage of dedicated resource is in reference to storage only (paragraph 26, page 9).

Examiner has reviewed the specification (OCR whole document) and could not find support for the additional limitations as claimed.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

5. Claims 1, 6, 7-12, 21-27 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1, 3-12, 21-27 recite the limitations, "the processor", "the exception". There is insufficient antecedent basis for this limitation in the claim. Since, multiple "processors" (plurality of processors) and "exceptions" (handling exceptions) exist in the claim, it is not clear which "processor" and "exception" is referred by the limitations in the claim. For example,

usage of "said" in front of a specific limitation refers to the specific limitation defined earlier in the claim.

Claim 3 recites the limitations, "the respective operating system". There is insufficient antecedent basis for this limitation in the claim. For example, it should be "the one of a plurality of operating systems".

Claims 4, 5, recites the limitations, "the processor", There is insufficient antecedent basis for this limitation in the claim. Since, multiple "processors" (plurality of processors) exist in the claim, it is not clear which "processor" is referred by the limitations in the claim.

Claim Objections

6. Claim 37 is objected to because of the following informalities:

Claim 37 mentions, "the first and second line cards", "a first and a second processors", "a first and a second exception", should be "the first line card and the second line card", "a first processor and a second processor", "a first exception and a second exception", respectively. For example, "a first and a second processors" is not limited to "a first processor and a second processor", but usage of second processors (set).

Appropriate correction is required.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-3, 21-23, are rejected under U.S.C. 103(a) as being unpatentable over Browning et al., 6,006,247, IBM (Hereinafter Browning-IBM) in view of Hartnett et al., 6,167,479, Unisys (Hereinafter Hartnett), O'Shea-Intel 6,611,911, Intel (Hereinafter O'Shea-Intel) and Endo et al., 6,615,303, Hitachi, Ltd, (Hereinafter Endo-Hitachi).

9. As per claims 1, 21, Browning-IBM teaches the following:

a method and a machine-readable medium that provides instructions for handling exceptions in a multiple processor system (e.g., col., 2, lines 40 –65, col., 4, lines 6 – 22, figure 1), comprising:

receiving an exception within a processor (e.g., col., 2, lines 40 –65) which is one of a plurality of processors of the multi-processor system (e.g., block 44, figure 2), wherein each processor in the multi- processor system shares a memory (e.g., usage of L1 and/or L2, figure 2, col., 4, lines 6 – 22);

wherein the memory includes a common interrupt handling vector address space shared by the plurality of the processors (e.g., col., 3, line 65 – col., 4, line 29),

executing one or more instructions at an address associated with the received exception within the common interrupt handling vector address space of the memory (e.g., col., 4, lines 46 – 65) wherein the number of instructions cause the processor to modify based on identification of the processor (e.g., block 44, figure 2) to execute interrupt handler (e.g., figure 2, block 44, col., 4, lines 35 – 46) and modifying execution flow of the exception (e.g., col., 6, lines 16 – 36).

However, Browning-IBM does not specifically mention about usage of a type of the exception and a dedicated interrupt handling vector address space.

Hartnett-Unisys discloses usage of a type of the exception and a dedicated interrupt handling vector address space (e.g., paragraphs 29 and 67).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Browning-IBM with the teachings of Hartnett-Unisys in order to facilitate usage of a type of the exception and a dedicated interrupt handling vector address space because the type would help provide information related to what kind of exception is present. The well-known concept of using a dedicated interrupt handling vector address space would enhance supporting processing of the exception.

However, Browning-IBM and Hartnett-Unisys do not specifically mention about memory within multiprocessor system.

O'Shea-Intel teaches memory within multiprocessor system (e.g., figure 1, col., 4, lines 1 – 18).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Browning-IBM and Hartnett-Unisys with the teachings of O'Shea-Intel in order to facilitate memory within multiprocessor system because the memory would help store information related to the processors executing information.

Browning-IBM, Hartnett-Unisys and O'Shea-Intel do not specifically mention about executing an interrupt handler located within one of a number of different interrupt handling vector address spaces.

Endo-Hitachi teaches executing an interrupt handler located within one of a number of different interrupt handling vector address spaces (e.g., figure 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Browning-IBM, Hartnett-Unisys and O'Shea-Intel with the teachings of Endo-Hitachi in order to facilitate executing an interrupt handler located within one of a number of different interrupt handling vector address spaces because the interrupt handler would help handle the interrupt. The well-known concept of using different interrupt handlers stored in the memory would help handle different types of interrupts. The processor would help process the exceptions / interrupts using the different interrupt handlers.

10. As per claims 2, 3, 22, 23, Browning-IBM, Hartnett-Unisys, O'Shea-Intel and Endo-Hitachi teach the claimed limitations as rejected above. Endo-Hitachi also teaches each processor in the multi-processor system executes one of a plurality of operating systems (e.g., figure 1) at least two of the operating systems are different (e.g., figure 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Browning-IBM, Hartnett-Unisys, O'Shea-Intel and Endo-Hitachi in order to facilitate each processor in the multi-processor system to execute one of a number of operating systems associated with one of the number of different interrupt handling vector address spaces because the processor would be able to use any operating system from the available multiple operating systems. Depending upon the operating system used by the processor would help the functionality provided by the operating system. The well-known concept of using associated interrupt handling space would help process the interrupt using the operating system handled by the processor.

11. Claims 4-5, 24-25, are rejected under U.S.C. 103(a) as being unpatentable over Browning-IBM, Hartnett-Unisys, O'Shea-Intel and Endo-Hitachi in view of Rose, 6,314,500 IBM (Hereinafter Rose-IBM) and Martonosi et al., 6,745,336 (Hereinafter Martonosi).

12. As per claims 4-5, 24-25, Browning-IBM, Hartnett-Unisys, O'Shea-Intel and Endo-Hitachi teach the claimed limitations as rejected above. However, Browning-IBM, Hartnett-Unisys, O'Shea-Intel and Endo-Hitachi do not specifically mention about reading a bit within an internal register and the register is not dedicated to determining the identification of the processor.

Rose-IBM teaches reading a bit of a register without having to access memory (e.g., col., 9, lines52 – 67).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Browning-IBM, Hartnett-Unisys, O'Shea-Intel and Endo-Hitachi with the teachings of Rose-IBM in order to facilitate reading a bit of a register without having to access memory because a bit within a register would provide information of the processor among the group of processors.

Browning-IBM, Hartnett-Unisys, O'Shea-Intel, Endo-Hitachi and Rose-IBM do not specifically mention about the usage of cache throttling register and a dedicated bit.

Martonosi discloses the concept of using the cache throttling register and a dedicated bit (e.g., paragraph 34).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Browning-IBM, Hartnett-Unisys, O'Shea-Intel, Endo-Hitachi and Rose-IBM with the teachings of Martonosi in order to facilitate using the cache

throttling register and a dedicated bit because the cache throttling register would provide its bits to store information for the processor among the group of processors.

13. Claims 6, 7, 26, 27, are rejected under U.S.C. 103(a) as being unpatentable over Browning-IBM, Hartnett-Unisys, O'Shea-Intel, Endo-Hitachi, Rose-IBM and Martonosi in view of Colley et al., 5,113,523, NCUBE Corporation (Hereinafter Colley - NCUBE) and Stracovsky et al., 6,539,440, Infineon (Hereinafter Stracovsky-Infineon).

14. As per claims 6, 7, 26, 27, Browning-IBM, Hartnett-Unisys, O'Shea-Intel, Endo-Hitachi, Rose-IBM and Martonosi teach the claimed limitations as rejected above.

However, Browning-IBM, Hartnett-Unisys, O'Shea-Intel, Endo-Hitachi, Rose-IBM and Martonosi do not specifically mention about communicating during an identification of the processor during initialization of the processor.

Colley – NCUBE teaches about of communicating during an identification of the processor during initialization of the processor (e.g., col., 27, lines 13 – 28).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Browning-IBM, Hartnett-Unisys, O'Shea-Intel, Endo-Hitachi, Rose-IBM and Martonosi with the teachings of Colley – NCUBE in order to facilitate communicating during an identification of the processor during initialization of the processor because the identification of the processor would help select the processor for processing information.

Browning-IBM, Hartnett-Unisys, O'Shea-Intel, Endo-Hitachi, Rose-IBM, Martonosi and Colley – NCUBE do not specifically mention about communications with a memory controller that is coupled between the processors in the multiple processor system and the same memory.

Stracovsky-Infineon teaches communications with a memory controller that is coupled between the processors in the multiple processor system and the same memory (e.g., col., 2, lines 17 – 36; col., 5, line 63 – col., 6, line 9).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Browning-IBM, Hartnett-Unisys, O'Shea-Intel, Endo-Hitachi, Rose-IBM, Martonosi and Colley – NCUBE in order to facilitate communications with a memory controller that is coupled between the processors in the multiple processor system and the same memory because the memory controller would help the processor to access the shared memory. The well-known concept of a memory usage would help provide information to the processors through the memory controller.

15. Claims 8-16 are rejected under U.S.C. 103(a) as being unpatentable over Browning-IBM, Hartnett-Unisys, O'Shea-Intel, Endo-Hitachi, Rose-IBM, Martonosi and Colley – NCUBE in view of Nota et. al, 5,805,790, Hitachi Ltd (Hereinafter Nota-Hitachi).

16. As per claims 8-10, 14, 15, Browning-IBM, O'Shea-Intel, Endo-Hitachi, Stracovsky-Infineon and Nota-Hitachi teach the claimed limitations as rejected above. However, Browning-IBM, O'Shea-Intel, Endo-Hitachi, Stracovsky-Infineon and Nota-Hitachi do not specifically mention about reading a bit within an internal register and the register is not dedicated to determining the identification of the processor.

Rose-IBM teaches reading a bit within an internal register (e.g., col., 9, lines52 – 67) and the register is not dedicated to determining the identification of the processor (e.g., col., 9, lines 52 – 67).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Browning-IBM, O'Shea-Intel, Endo-Hitachi, Stracovsky-Infineon and Nota-Hitachi with the teachings of Rose-IBM in order to facilitate reading a bit within an internal register and the register is not dedicated to determining the identification of the processor because a bit within a register would provide information of the processor among the group of processors. The well-known concept of using a register not dedicated for determining the identification of the processor would help the register to be used for determining other information besides only determining the identification of the processor.

17. As per claims 11 and 16, Browning-IBM, O'Shea-Intel, Endo-Hitachi, Stracovsky-Infineon, Rose-IBM and Nota-Hitachi teach the claimed limitations as rejected above.

However, Browning-IBM, O'Shea-Intel, Endo-Hitachi, Stracovsky-Infineon, Rose-IBM and Nota-Hitachi do not specifically mention about determining the identification of the processor during initialization of the processor.

Colley – NCUBE teaches determining the identification of the processor during initialization of the processor (e.g., col., 27, lines 13 – 28).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Browning-IBM, O'Shea-Intel, Endo-Hitachi, Stracovsky-Infineon, Rose-IBM and Nota-Hitachi with the teachings of Colley – NCUBE in order to

facilitate determining the identification of the processor during initialization of the processor because the identification of the processor would help select the processor for processing information. The well-known concept of using a processor for initialization would help initialize the processor (itself) and the system.

18. As per claim 12, Browning-IBM, Hartnett-Unisys, O'Shea-Intel, Endo-Hitachi, Rose-IBM, Martonosi and Colley – NCUBE disclose the claimed limitations as discloses above.

Browning-IBM, Hartnett-Unisys, O'Shea-Intel, Endo-Hitachi, Rose-IBM, Martonosi and Colley – NCUBE do not specifically mention about the first processor is to execute a first operating system and the second processor is to execute a second operating system.

Nota-Hitachi teaches the first processor is to execute a first operating system (e.g., col., 2, lines 24 – 29, figure 1) and the second processor is to execute a second operating system (e.g., col., 2, lines 24 – 29, figure 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Browning-IBM, Hartnett-Unisys, O'Shea-Intel, Endo-Hitachi, Rose-IBM, Martonosi and Colley – NCUBE with the teachings of Nota-Hitachi in order to facilitate the first processor is to execute a first operating system and the second processor is to execute a second operating system because the first processor would help support the first operating system and the second processor would help support the second operating system. Having multiple processors would help support multiple operating systems. Having multiple different operating systems would help support functionality of all different operating systems supported by the system.

19. As per claim 13, Browning-IBM, Hartnett-Unisys, O'Shea-Intel, Endo-Hitachi, Rose-IBM, Martonosi, Colley – NCUBE and Nota-Hitachi teach the claimed limitations as rejected above. Endo-Hitachi also teaches executing different operating systems associated with one of the number of different interrupt handling vector address spaces (e.g., figure 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Browning-IBM, Hartnett-Unisys, O'Shea-Intel, Endo-Hitachi, Rose-IBM, Martonosi and Colley – NCUBE with the teachings of Nota-Hitachi in order to facilitate executing different operating systems associated with one of the number of different interrupt handling vector address spaces because different interrupt handlers would help handle interrupts for different operating systems. The well-known concept of using different interrupt handlers stored in the memory would help handle different types of interrupts depending upon the operating system used. The processor would help process the exceptions / interrupts using the different interrupt handlers.

20. Claim 33 is rejected under U.S.C. 103(a) as being unpatentable over Browning-IBM, Hartnett, O'Shea-Intel and Endo-Hitachi in view of Venkitakrishnan, 6,263,415.

21. As per claim 33, Browning-IBM, Hartnett, O'Shea-Intel and Endo-Hitachi teach the claimed limitations rejected under claim 2. However, Browning-IBM, Hartnett, O'Shea-Intel and Endo-Hitachi do not specifically mention about usage of two different networks.

Venkitakrishnan discloses the concept of using two different networks (e.g., paragraphs 8-10).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Browning-IBM, Hartnett, O'Shea-Intel and Endo-Hitachi with the teachings of Venkitakrishnan in order to facilitate using two different networks because the different networks would help support handling of information for the devices located on both type of networks.

22. Claim 34-35 are rejected under U.S.C. 103(a) as being unpatentable over Browning-IBM, Hartnett, O'Shea-Intel and Endo-Hitachi and Venkitakrishnan in view of Kidder et al., 6,880,086 (Hereinafter Kidder).

23. As per claim 34, Browning-IBM, Hartnett, O'Shea-Intel and Endo-Hitachi teach the claimed limitations rejected under claim 33. However, Browning-IBM, Hartnett, O'Shea-Intel, Endo-Hitachi and Venkitakrishnan do not specifically mention about usage line cards and control cards for routing traffic.

Kidder discloses the concept of usage line cards and control cards for routing traffic (e.g., paragraphs 14, 186, 225, 247, 274).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Browning-IBM, Hartnett, O'Shea-Intel, Endo-Hitachi and Venkitakrishnan with the teachings of Kidder in order to facilitate using line cards and control card for routing traffic because the line cards and control card would enhance supporting communication between devices over the networks. The routing of traffic using the cards would help support handling of information for the devices located on the networks.

24. As per claim 35, Browning-IBM, Hartnett, O'Shea-Intel, Endo-Hitachi, Venkitakrishnan and Kidder teach the claimed limitations as rejected above. Kidder also discloses usage of a network provider and service provider (e.g., paragraphs 14, 186, 225, 247, 274).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Browning-IBM, Hartnett, O'Shea-Intel, Endo-Hitachi and Venkitakrishnan with the teachings of Kidder in order to facilitate usage of a network provider and service provider because the provides would enhance supporting service and network resources to the devices present on the networks. The routing of traffic using the cards would help support handling of information for the devices located on the networks.

25. Claim 36 is rejected under U.S.C. 103(a) as being unpatentable over Browning-IBM, Hartnett, O'Shea-Intel, Endo-Hitachi and Venkitakrishnan and Kidder in view of Schuster et al., 6,856,616 (Hereinafter Schuster).

26. As per claims 36-39, Browning-IBM, Hartnett, O'Shea-Intel, Endo-Hitachi and Venkitakrishnan and Kiddeteach the claimed limitations as rejected above. However, Browning-IBM, Hartnett, O'Shea-Intel, Endo-Hitachi and Venkitakrishnan and Kidde do not specifically mention about handling of provisioning and configuration.

Schuster discloses the concept of handling of provisioning and configuration (e.g., paragraph 13).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Browning-IBM, Hartnett, O'Shea-Intel, Endo-Hitachi, Venkitakrishnan and Kidderwith the teachings of Schuster in order to facilitate handling of

provisioning and configuration because the provisioning and configuration would enhance supporting configuration and provisioning of service and network resources to the devices present on the networks. The routing of traffic using the cards would help support handling of information for the devices located on the networks.

Conclusion

27. The prior art made of record (forms PTO-892 and applicant provided IDS cited arts) and not relied upon is considered pertinent to applicant's disclosure. For example, Ronkka et al., 6,631,394, also teaches the concept of handling exceptions/interrupts using common interrupt/exception handler for different types of operating systems.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Haresh Patel whose telephone number is (571) 272-3973. The

examiner can normally be reached on Monday, Tuesday, Thursday and Friday from 10:00 am to 8:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Follansbee can be reached on (571) 272-3964. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Haresh Patel

August 21, 2005

JOHN FOLLANSBEE
SUPERVISORY PATENT EXAMINER
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